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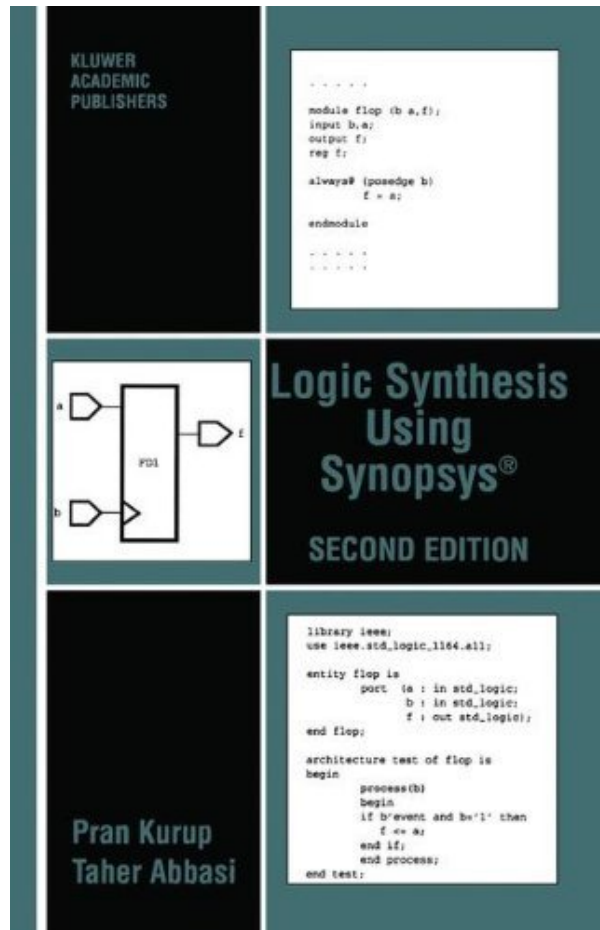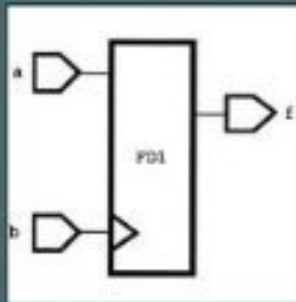

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```
. . . . .
module flop (b a,f);
input b,a;
output f;
reg f;

always@ (posedge b)
        f = a;

endmodule

. . . . .
. . . . .
```

Logic Synthesis Using Synopsys®

SECOND EDITION

FD1

a

b

f

```
library ieee;
use ieee.std_logic_1164.all;

entity flop is
        port (a : in std_logic;
              b : in std_logic;
              f : out std_logic);
end flop;

architecture test of flop is
begin
        process(b)
        begin
        if b'event and b='1' than
           f <= a;
        end if;
        end process;
end test;
```

Pran Kurup
Taher Abbasi

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Logic Synthesis Using Synopsys®, Second Edition is for anyone who hates reading manuals but would still like to learn logic synthesis as practised in the real world. Synopsys Design Compiler, the leading synthesis tool in the EDA marketplace, is the primary focus of the book. The contents of this book are specially organized to assist designers accustomed to schematic capture-based design to develop the required expertise to effectively use the Synopsys Design Compiler. Over 100 `Classic Scenarios' faced by designers when using the Design Compiler have been captured, discussed and solutions provided. These scenarios are based on both personal experiences and actual user queries. A general understanding of the problem-solving techniques provided should help the reader debug similar and more complicated problems. In addition, several examples and dc_shell scripts (Design Compiler scripts) have also been provided.

Logic Synthesis Using Synopsys®, Second Edition is an updated and revised version of the very successful first edition.

The second edition covers several new and emerging areas, in addition to improvements in the presentation and contents in all chapters from the first edition. With the rapid shrinking of process geometries it is becoming increasingly important that `physical' phenomenon like clusters and wire loads be considered during the synthesis phase. The increasing demand for FPGAs has warranted a greater focus on FPGA synthesis tools and methodology. Finally, behavioral synthesis, the move to designing at a higher level of abstraction than RTL, is fast becoming a reality. These factors have resulted in the inclusion of separate chapters in the second edition to cover Links to Layout, FPGA Synthesis and Behavioral Synthesis, respectively. Logic Synthesis Using Synopsys®, Second Edition has been written with the CAD engineer in mind. A clear understanding of the synthesis tool concepts, its capabilities and the related CAD issues will help the CAD engineer formulate an effective synthesis-based ASIC design methodology. The intent is also to assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

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